FORM PTO-1449	SERIAL NO. 10/736,350	CASE NO. 13309US04
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	FILING DATE December 15, 2003	GROUP ART UNT ~~to be assigned~~ 2827
(use several sheets if necessary)	APPLICANT(S): Mortieza Cyrus Afghahi	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS/ SUBCLASS	FILING DATE
TP		3,609,710	09/28/1971	Browne	340/173	05/29/1969
TP		5,475,633	12/12/1995	Mehalel	365/154	06/01/1994

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES	NO

EXAMINER INITIAL		OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)
TP		Miyatake, H. et al., "A Design For High-Speed Low-Power CMOS Fully Parallel Content-Addressable Memory Macros", *IEEE Journal of Solid-State Circuits*, IEEE Inc., Vol. 36, No. 6, June 2001, pages 956-968
		Noda, K. et al., "A 1.9-μm^2 Loadless CMOS Four-Transistor SRAM Cell in a 0.18-μm Logic Technology", Electron Devices Meeting, 1998. *IEDM '98 Technical Digest.*, International San Francisco, CA, 1998, pages 643-646
		Grosspietsch, K.E., "Associative Processors and Memories: A Survey", *IEEE Micro*, Vol. 12, No. 3, June 1, 1992, pages 12-19
		"High Performance Static Content Addressable Memory Cell", *IBM Technical Disclosure Bulletin*, IBM Corp., Vol. 32, No. 3A, August 1, 1989 page 478
↓		Fitchen, Franklin C., "Transistor Circuit Analysis And Design", *D. Van Nostrand Co.* (1960), pages 304-314

EXAMINER Trong Phan	DATE CONSIDERED 3/18/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.